Intra-Chip Free-Space Optical Interconnect: System, Device, Integration and Prototyping

by

Berkehan Ciftcioglu

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Supervised by
Professor Hui Wu

Department of Electrical and Computer Engineering
Arts, Sciences and Engineering
Edmund A. Hajim School of Engineering and Applied Sciences
University of Rochester
Rochester, New York

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Abstract

As both the number and performance of microprocessor cores continue to increase with technology scaling, communication between processor cores and memory/processor interfaces will demand larger I/O bandwidth and better signal integrity, requiring a fundamental change in the intra- and inter-chip electrical interconnect architectures. Optical interconnect, as a promising alternative, exhibits inherent advantages in loss, delay, and bandwidth; mitigating the limitations of its electrical counterpart and potentially generating significant performance gains and energy savings. However, current intra-chip optical interconnect schemes, utilizing either packet switching or wavelength division multiplexing (WDM) with a bus architecture, poses significant challenges in latency, energy efficiency, routing, and fabrication.

This thesis presents a new fully-distributed 3-D integrated intra-chip free-space optical interconnect (FSOI) system, leveraging mature photonics devices such as semiconductor lasers and photodiodes, optics technologies such as micro-lenses and mirrors, and 3-D integration. This interconnect system provides point-to-point free-space optical links between any two communication nodes to construct an all-to-all intra-chip communication network with little or no arbitration. Therefore, it has significant networking advantages over other optical and electrical interconnect systems. Unlike other electrical and waveguide-based optical interconnect systems, FSOI provides low latency and high energy efficiency, eliminating the delays and energy consumption associated with packet switching, routing, and buffering of the conventional electrical

and other optical networks. Especially, it reduces the latency to its ultimate lower bound, reducing the idling time of cores during data package transmission, which is the major bottleneck in the real-world performance of multi-core processors. FSOI also reduces the interconnect loss and provides no bandwidth degradation for long distance transmission, achieving large bandwidth density. It eliminates the losses associated with waveguide crossings in large-scale systems and reduces the routing complexity significantly. In addition, it eliminates the crosstalk between long waveguides, improving the signal integrity. Finally, improved signal integrity of FSOI simplifies the electronics into a conventional transceiver and eliminating the need for advanced signal processing techniques or equalization.

An FSOI system is evaluated based on the real device parameters, predictive technology models and International Roadmap of Semiconductor's predictions. A single FSOI link achieves 10-Gbps data rate with 0.5-pJ/bit energy efficiency and less than 10^{-12} bit-error-rate (BER). A system using this individual link can provide scalability up to 36 nodes, providing 10-Tbps aggregate bandwidth. Comparisons with respect to a WDM-based waveguide interconnect system show that FSOI achieves better energy efficiency and lower latency. Network simulations on a 16-core microprocessor using the proposed FSOI system instead of electrical mesh networks has been shown to speed up by 1.46 times while reducing the energy consumption by 33%.

As a part of the development of a 3-D integrated FSOI system, operating at 850 nm with a 10-Gbps data rate per optical link, the photonics devices and optical components are individually designed and fabricated. The focus in the system is the implementation of high performance and efficiency photodiodes due to the difficulties in the implementation of high efficiency and large bandwidth laser diodes. The metal-semiconductor-metal (MSM) structure is chosen over p-i-n ones to reduce parasitic capacitance per area, to allow less stringent micro-lens-to-PD alignment for efficient light coupling, while achieving reasonably good bandwidth and responsivity. A novel

germanium MSM photodiode, in which an amorphous silicon (a-Si) layer is added on top of the undoped germanium substrate, is introduced. The a-Si under the Ti/Au contacts serves as a barrier enhancement layer and mitigates the low Schottky barrier height for holes due to fermi level pinning, hence reducing the dark current. In addition, the a-Si in the active region passivates the surface states, thus preventing low-frequency gain due to charge accumulation and image force lowering of the barrier, and improving the bandwidth. A fabricated PD using this technique achieves a 3-dB bandwidth over 13 GHz with 0.315-A/W responsivity and 1.7-nAμm^2 dark current density.

The micro-lenses are fabricated on a fused silica substrate based on the photoresist melt-and-reflow technique photoresist. Then, the spherical resist patterns are transferred into fused silica substrate via dry etching. The measured focal length of a 220-μm aperture size micro-lens is 350-μm away from the backside of the substrate. The vertical-cavity surface-emitting lasers are fabricated on a commercial molecular beam epitaxially (MBE) grown GaAs wafer. The fabricated 6-μm aperture size VCSEL can achieve 0.65-mW optical power at 1.5-mA forward bias current with a threshold current of 0.48 mA. The slope efficiency is measured as 0.67-A/W and the bandwidth is more than 4 GHz.

Three prototypes are built integrating these components via non-conductive epoxy and wirebonding. The first prototype, built on a printed circuit board (PCB) using commercial VCSEL arrays, achieves more than 10-GHz bandwidth, limited by the VCSEL, and 5-dB transmission loss at 1-cm distance. The crosstalk was below -25 dB up to 2.6 cm. The second chip-scale prototype on a germanium carrier chip achieves 4-dB transmission loss at 1 cm and 3.3-GHz bandwidth, mainly limited by the 5-GHz bandwidth of the commercial VCSEL chip. The final prototype uses all fabricated components integrated on a PCB. The prototype achieves 9-dB transmission loss at 3-cm distance and 4.4-GHz bandwidth.